in a direction of the <110> axis with respect to a single semiconductor substrate. This is different than what is disclosed and suggested by Chang.

First, as the Examiner notes, Chang does not disclose that the concentration of the impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region. As a result, the Examiner states that "the ratio of impurity concentrations in these two regions in Chang's MOSFET is substantially close or within the range of 1/100 to 1/10." Furthermore, the Examiner also asserts that, in "general, the impurity concentrations of the doped regions are well recognized variables of importance, their specific amounts and the ratio between them are subjected to routine experimentation and optimization."

Applicants submit, however, that there is no disclosure in Change indicating that the impurity in the alleged channel forming region of Chang is 1/100 to 1/10 of that in the impurity region, and *the Examiner has failed to cite anywhere within Chang wherein there is such a disclosure or suggestion.*

This is an advantage of the present invention over the prior art. More specifically, when the impurity remains in the channel region, there are various problems such as lowering of the on current and lowering the mobility (see present application, page 3, lines 13-27). The semiconductor device of the present invention, as recited in Claim 1, is intended to solve these problems. Accordingly, it is very important to reduce the impurity in the channel region to the degree specified by the claimed invention. The claimed limitation is not one of routine experimentation and optimization because of these specific problems and the attempts to solve them. Hence, this is a clear distinguishing feature of the claims of the present application over Chang et al.

Additionally, Claim 1 has been amended to recite the further feature of wherein the impurity is introduced from a direction of the <110> axis with respect to a single semiconductor substrate. This is another advantage of the present invention. In particular, if the impurity is introduced in the

direction of the <110> axis and since the smallest atom density is on the {110} face, the impurity ion can be introduced to a deeper position with smaller damage (see e.g. page 4, lines 11-13). Therefore, crystallinity in the vicinity of a surface of the single crystalline semiconductor substrate is not be destroyed by the collision ions (in contrast, see page 2, line 28 through page 3, line 3 of the present application).

Applicants believe that Chang does not disclose or suggest this feature and therefore does not have this advantage of the present invention.

Accordingly, it is respectfully submitted that the claims of the present application are patentably distinguishable over the cited reference and should now be allowed.

In the Notice of Draftsman Patent Drawing Review for the Office Action of August 6, 1999, the Draftsman states that the solid black shading of Fig. 9 is not permitted. Accordingly, Applicants are submitting herewith a substitute Fig. 9. In the original Fig. 9, the solid black material only shows an outside of an integrated circuit (IC). In amended Fig. 9, the black hatching is removed from the middle member of Fig. 9. The middle member is an example of the integrated circuit (IC) 18. It is believed that this will overcome the draftsman's objection to the drawings. As it is believed that no new matter is being added, it is requested that this amendment be entered, and the objection withdrawn.

It is respectfully submitted that this application is now in a condition for allowance and should be allowed. Please charge our deposit account 50/1039 for any fee due for the new claims.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date:

Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
200 West Adams Street
Suite 2850
Chicago, Illinois 60606
(312) 236-8500